

Claims

- [c1] A method for forming a complementary metal oxide semiconductor (CMOS) device, comprising:
providing a semi conducting substrate having a gate with a source and a drain region;
depositing a gate dielectric layer on said semi conducting substrate;
depositing a metal gate layer;
capping said metal gate layer with a silicide formed on top of said gate; and
performing conventional formation of said CMOS device.
- [c2] The method of claim 1 wherein said metal gate layer comprises a metal or metal alloy.
- [c3] The method of claim 1 wherein said gate dielectric layer comprises Al_2O_3 , HfO_2 , ZrO_3 , Y_2O_3 , La_2O_3 , SiO_2 , nitrided SiO_2 , Si_3N_4 , silicates, metal oxides or mixtures and nitrogen additions thereof.
- [c4] The method of claim 1 wherein said metal gate layer comprises Ru, Rh, W, Mo, Re, Ir, Pt, TiN, TaN, or TaSiN.
- [c5] The method of claim 1 further comprising capping said metal gate layer with CoSi_2 , NiSi, TiSi_2 , WSi_2 , TaSi_2 , MoSi_2 , PdSi, PtSi or mixtures thereof.

- [c6] The method of claim 1 further comprising capping said metal gate layer with a NiSi, CoSi₂, TiSi₂, or WSi₂ silicide.
- [c7] A method of forming a gate metal silicide for CMOS devices on a semiconductor wafer comprising:
depositing a gate dielectric layer on said wafer;
depositing a metal gate layer over said gate dielectric layer;
depositing a silicon layer over said metal gate layer;
patterning said wafer to form gates;
depositing sidewall spacer material;
etching said wafer to form sidewall spacers;
performing source and drain ion implantation; and
annealing said wafer at a temperature sufficient to activate implantation species and form a silicide of said gate silicon layer.
- [c8] The method of claim 7 wherein depositing said silicon layer comprises depositing a silicon layer thinner than said metal gate layer such that the entire polysilicon layer is consumed in the silicide formation.
- [c9] The method of claim 7 wherein depositing said silicon layer comprises depositing a silicon layer thicker than said metal gate layer such that at least a portion of said metal gate and polysilicon layers are consumed in the silicide formation.
- [c10] The method of claim 9 further comprising forming a third silicide on said polysilicon layer.

- [c11] The method of claim 10 comprising forming said third silicide of CoSi_2 , NiSi , WSi_2 , TiSi_2 , PtSi , and PdSi .
- [c12] A method of forming a gate metal silicide for CMOS devices on a semiconductor wafer prior to gate definition, comprising:
depositing a gate dielectric layer on said wafer;
depositing a gate metal layer over said gate dielectric layer;
depositing a silicon layer over said gate metal layer;
annealing said wafer to form silicide;
patterning said wafer to form gates after said annealing process;
and
depositing an oxide as a sidewall spacer; and
annealing said wafer at a temperature sufficient to activate implantation species.
- [c13] The method of claim 12 wherein depositing said metal layer comprises depositing Co, W, Mo, Ru, Rh, Re, or Ir.
- [c14] The method of claim 13 further comprising forming a second silicide layer of a metal different than said gate metal layer over said silicon layer, said second silicide layer comprising Co, W, Ti, Ta, Ni, or Mo.
- [c15] The method of claim 12 further comprising depositing a silicide metal layer over said gate metal layer.
- [c16] The method of claim 12 further comprising depositing a barrier layer over said metal layer to prevent silicide formation of said

gate metal layer.

[c17] The method of claim 16 wherein said barrier layer comprises graded nitride compositions comprising TiN, TaSiN, WN, TiAlN or TaN.

[c18] A method of forming a replacement gate structure for CMOS devices on a semiconductor wafer, comprising:
providing a patterned gate structure having a sacrificial gate dielectric, sidewall spacers, shallow trench isolation, source and drain ion implantation regions, and a polysilicon layer over said gate dielectric;
depositing a Si_3N_4 / SiO_2 bilayer surrounding the gate region;
removing said polysilicon layer and sacrificial gate dielectric;
growing said gate dielectric over said patterned gate structure;
depositing a metal gate liner over said gate dielectric;
depositing a silicon layer over said metal liner;
planarizing structure using chemical mechanical polishing (CMP);
forming a silicide metal layer;
annealing said gate structure; and
removing any unreacted metal.

[c19] The method of claim 18 further comprising depositing a silicide barrier liner over said metal gate liner, and depositing a silicon gate fill over said barrier.

[c20] A method of forming an interconnect on a dual metal

replacement gate structure for connection of nFET and pFET gates of a CMOS device on a semiconductor wafer, comprising:

- providing a patterned gate structure having a sacrificial gate dielectric, sidewall spacers, shallow trench isolation, source and drain ion implantation regions, and a first and a second doped polysilicon regions over said sacrificial gate dielectric;
- removing said first N⁺ doped polysilicon region and a portion of said sacrificial gate dielectric;
- depositing a first dielectric;
- depositing a first nFET metal in place of said first N⁺ doped polysilicon region;
- depositing an undoped poly over said first nFET metal;
- performing chemical mechanical polishing on said wafer;
- removing said second P⁺ doped polysilicon region and a portion of said sacrificial gate dielectric;
- depositing a second dielectric;
- depositing a second pFET metal in place of said second P⁺ doped polysilicon region;
- depositing an undoped poly over said second pFET metal;
- performing chemical mechanical polishing on said wafer;
- performing an etch on said first and second metals between said first and second polysilicon regions;
- depositing a blanket polysilicon layer over said wafer;
- planarizing said deposited polysilicon;
- depositing a metal over said polysilicon layer; and

performing silicidation of said metal .